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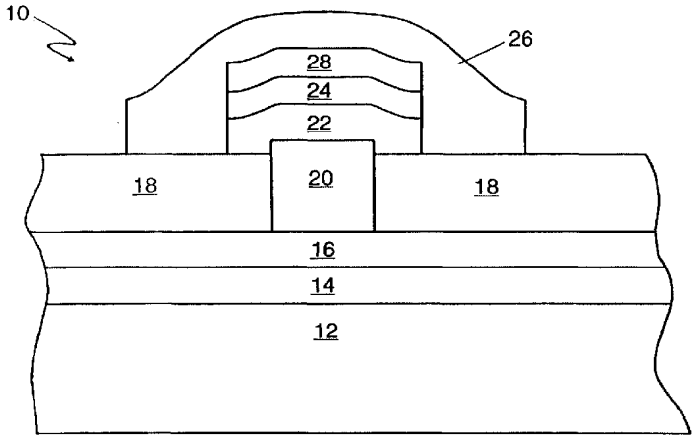
(54) Title: METAL-TO-METAL ANTIFUSE EMPLOYING CARBON-CONTAINING ANTIFUSE MATERIAL



(57) Abstract: A metal-to-metal antifuse is disposed between two metal interconnect layers in an integrated circuit. An insulating layer is disposed above a lower metal interconnect layer. The insulating layer includes a via formed therethrough containing a tungsten plug in electrical contact with the lower metal interconnect layer. The tungsten plug forms a lower electrode of the antifuse. The upper surface of the tungsten plug is planarized with the upper surface of the insulating layer. In a first embodiment, an antifuse material layer comprising amorphous carbon, amorphous carbon doped with hydrogen or fluorine, or amorphous silicon carbide is disposed above the upper surface of the tungsten plug. A layer of a barrier metal disposed over the antifuse material layer forms an upper electrode of the antifuse. An oxide or tungsten hard mask provides high etch selectivity and the possibility to etch barrier metals without affecting the dielectric constant value and mechanical properties of the antifuse material. In a second embodiment, a layer of barrier material is disposed between the top surface of the tungsten plug and the antifuse material layer. An adhesion-promoting layer may be used where amorphous carbon is used as the antifuse material layer.

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METAL-TO-METAL ANTIFUSE EMPLOYING CARBON-CONTAINING ANTIFUSE MATERIAL

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of the date of United States Patent Application No. 09/972,825, filed 02 October 2001.

BACKGROUND

The present application relates to antifuses, and more particularly, to metal-to-metal antifuses fabricated using carbon-containing antifuse layers.

Metal-to-metal antifuses are well known in the art. These devices are formed above a semiconductor substrate, usually between two metal interconnect layers in an integrated circuit and comprises an antifuse material layer sandwiched between a pair of lower and upper conductive electrodes, each electrode in electrical contact with one of the two metal interconnect layers.

Numerous materials have been proposed for use as antifuse material layers in above-substrate antifuses. Such materials include amorphous silicon or an alloy thereof, poly silicon, crystalline carbon, silicon, germanium, chalcogenide elements.

SUMMARY

A metal-to-metal antifuse is disposed between two metal interconnect layers in an integrated circuit. An insulating layer is disposed above a lower metal interconnect layer. The insulating layer includes a via formed therethrough containing a tungsten plug in electrical contact with the lower metal interconnect layer. The tungsten plug forms a lower electrode of the antifuse. The upper surface of the tungsten plug is planarized with the upper surface of the insulating layer. In a first embodiment, an antifuse material layer comprising a material selected from the group including amorphous carbon, amorphous carbon doped with hydrogen or fluorine, and amorphous silicon carbide is disposed above the upper surface of the tungsten plug. Where the antifuse material layer comprises amorphous carbon, amorphous carbon doped with hydrogen or fluorine, an adhesion-promoting layer of a material such as SiN or SiC may be provided at the interfaces of the antifuse material layer and the other layers in the structure. A barrier metal layer disposed over the antifuse material

layer forms an upper electrode of the antifuse. In a second embodiment, a barrier metal layer is also disposed between the top surface of the tungsten plug and the antifuse material layer.

BRIEF DESCRIPTION OF THE FIGURES

Referring now to the figures, wherein like elements are numbered alike:

FIG. 1 is a cross-sectional view of a first illustrative antifuse;

FIG. 2 is a cross-sectional view of a second illustrative antifuse;

FIG. 3 is a cross-sectional view of a third illustrative antifuse;

FIG. 4 is a cross-sectional view of a fourth illustrative antifuse;

FIGS. 5A through 5C are cross-sectional views of the antifuse of FIG. 1 showing the structure existing at selected points in the fabrication process;

FIGS. 6A through 6C are cross-sectional views of the antifuse of FIG. 2 showing the structure existing at selected points in the fabrication process;

FIGS. 7A through 7C are cross-sectional views of the antifuse of FIG. 3 showing the structure existing at selected points in the fabrication process; and

FIGS. 8A through 8C are cross-sectional views of the antifuse of FIG. 4 showing the structure existing at selected points in the fabrication process.

DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description is illustrative only and not in any way limiting. Other embodiments will readily suggest themselves to such skilled persons.

The metal-to-metal antifuses are disposed between two metal interconnect layers that lie above and are insulated from the semiconductor substrate in an integrated circuit. An insulating layer is disposed above a lower metal interconnect layer. The insulating layer includes a via formed therethrough containing a tungsten plug in electrical contact with the lower metal interconnect layer. The tungsten plug forms a lower electrode of the antifuse. The upper surface of the tungsten plug is planarized with the upper surface of the insulating layer.

Referring first to FIG. 1, a cross-sectional view shows a first illustrative metal-to-metal antifuse 10. In the embodiment shown in FIG. 1, substrate 12 is shown covered by insulating layer 14 and metal interconnect layer 16. Persons of ordinary skill in the art will realize that FIG. 1 is merely illustrative and that metal interconnect layer 16 need not be the first metal interconnect layer in a multi-level metal integrated circuit.

Insulating layer 18, comprising, for example, deposited silicon dioxide having a thickness from between about 400 nanometers (nm) to about 1,000 nm, is disposed above metal interconnect layer 16 and includes a tungsten plug 20 formed in a via therethrough and electrically coupled to metal interconnect layer16. As is known in the art, the upper surfaces of insulating layer 18 and tungsten plug 20 may be planarized to provide a relatively flat surface upon which to fabricate antifuse 10. Alternatively, tungsten plug 20 may be raised above the surface of the insulating layer 18 by performing planarization using CMP techniques or by performing a plasma oxide etch after planarization.

In the embodiment of FIG. 1, an antifuse material layer 22 is disposed over tungsten plug 20. The antifuse material layer 22 may comprise a material selected from the group including amorphous carbon, amorphous carbon doped with hydrogen or fluorine, and amorphous silicon carbide and may have a thickness of about 2.5 nm to about 1,000 nm. In addition, combinations of the materials as disclosed herein may be used for the antifuse material layer 22. The amorphous carbon, and combinations thereof, are disposed over the tungsten plug 20 by a source gas, preferably acetylene gas (C_2H_2)

For example, the antifuse material layer 22 may be formed from amorphous carbon, amorphous carbon doped with fluorine or hydrogen, or amorphous silicon carbide having a thickness of between about 10 nm to about 80 nm. Where antifuse material layer 22 is formed from amorphous carbon doped with hydrogen, the hydrogen doping should be from about 1 atomic percent to about 40 atomic percent. Where antifuse material layer 22 is formed from amorphous carbon doped with fluorine, the fluorine doping should be from about 0.5 atomic percent to about 20 atomic percent. Where antifuse material layer 22 is formed from silicon carbide, the percentage of carbon atoms in the composition should be greater than 50%.

Antifuse material layer 22 may also be formed from a combination of layers. A first example is a layer of amorphous silicon carbide having a thickness of about 2.5 nm, a layer of amorphous carbon having a thickness of between about 10 nm and about 80 nm, and a layer of amorphous silicon carbide having a thickness of about 2.5 nm. A second example is a layer of amorphous silicon nitride having a thickness of about 2.5 nm, a layer of amorphous carbon having a thickness of between about 10 nm and about 80 nm, and a layer of amorphous silicon nitride having a thickness of about 2.5 nm.

When the antifuse material layer 22 comprises amorphous carbon or doped amorphous carbon, a thin (e.g., 2.5 nm) adhesion-promoting layer of SiN or SiC (not shown

in FIG. 1) is disposed below the antifuse material layer 22 and above the antifuse material layer 22 to promote adhesion between that layer and the adjoining layers in the antifuse structure. For purposes of this disclosure, antifuse material layers comprising amorphous carbon or doped amorphous carbon shall be construed to include such adhesion-promoting layers as a part of their structure.

A barrier metal layer 24 such as Ta, TaN, TaC, Ti, TiC, or TiN having a thickness of about 25 nm to about 200 nm is disposed over the antifuse material layer forming an upper electrode of the antifuse. In a second embodiment to be disclosed herein, an additional lower barrier metal layer is disposed between the top surface of the tungsten plug and the antifuse material layer 22. In the embodiment illustrated in FIG. 1, an oxide layer 28 is deposited over the barrier metal layer 24. A layer of photoresist is deposited on the oxide layer and then oxide layer is etched.

Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. The oxide layer 28 protects the antifuse material layer 22 from being removed during the photoresist stripping step. Since Al, Ti, Ta, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. Since the tungsten layer is thin, only a thin layer of photoresist is required to pattern the hard mask. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched in reactive ion etch (RIE) with an SF6 chemistry. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22.

In the embodiment illustrated in FIG. 1, a metal interconnect layer 26 is disposed over the barrier metal layer 24. In a variation of the embodiment of FIG.1, an insulating layer may be formed over barrier metal layer 24 and metal interconnect layer 26 will make contact with barrier metal layer 24 through a contact via formed in the insulation layer.

Referring now to FIG. 2, a cross-sectional view shows a second illustrative metal-to-metal antifuse 30. The embodiment illustrated in FIG. 2 is similar to the embodiment illustrated in FIG. 1, and structures in the embodiment of FIG. 2 corresponding to structures

in FIG. 1 will be identified by the same reference numerals. Also, unless otherwise noted, persons of ordinary skill in the art will appreciate that the materials and thicknesses of the various layers will be similar to those disclosed with respect to the embodiment of FIG. 1.

In the embodiment shown in FIG. 2, substrate 12 is shown covered by insulating layer 14 and metal interconnect layer 16. As was the case with the embodiment illustrated in FIG. 1, persons of ordinary skill in the art will realize that FIG. 2 is merely illustrative and that metal interconnect layer 16 need not be the first metal interconnect layer in a multi-level metal integrated circuit.

Insulating layer 18, comprising, for example, deposited silicon dioxide, is disposed above metal interconnect layer 16 and includes a tungsten plug 20 formed in a via therethrough and electrically coupled to metal interconnect layer 16. As is known in the art, the upper surfaces of insulating layer 18 and tungsten plug 20 may be planarized to provide a relatively flat surface upon which to fabricate antifuse 30. Alternatively, tungsten plug 20 may be raised above the surface of the insulating layer 18 by performing planarization using CMP techniques or by performing a plasma oxide etch after planarization.

As previously mentioned, the embodiment of the invention of FIG. 2 includes an additional barrier metal layer 32 disposed between the top surface of the tungsten plug and the antifuse material layer 22. Antifuse material layer 22 is the same as that disclosed with respect to the embodiment of FIG. 1.

A barrier metal layer 24 such as Ta, TaN, TaC, Ti, TiC, or TiN having a thickness of about 25 nm to about 200 nm is disposed over the antifuse material layer forming an upper electrode of the antifuse 30 of FIG. 2. In the embodiment illustrated in FIG. 2, an oxide layer 28 is deposited over the barrier metal layer 24. A layer of photoresist is deposited on the oxide layer and then oxide layer is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. The oxide layer 28 protects the antifuse material layer 22 from being removed during the photoresist stripping step. Since Al, Ti, Ta, TaC, TiC, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. Since the tungsten layer is thin, only a thin layer of photoresist is required to pattern the hard mask. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched in reactive

ion etch (RIE) with an SF6 chemistry. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22.

Another difference between the embodiments of FIGS. 1 and 2 is that an additional insulating layer 34, that may comprise a deposited layer of silicon dioxide having a thickness of about 100 nm to about 200 nm may be employed over the structure including barrier metal layer 32, antifuse material layer 22, and barrier metal layer 24, as shown in FIG. 2. Metal interconnect layer 26 is disposed over the insulating layer 34 and contacts barrier metal layer 24 through a via formed therethrough.

Referring now to FIG. 3, a cross-sectional view shows a third illustrative metal-to-metal antifuse 50. The embodiment illustrated in FIG. 3 is similar to the embodiment illustrated in FIG. 1, and structures in the embodiment of FIG. 3 corresponding to structures in FIG. 1 will be identified by the same reference numerals. Also, unless otherwise noted, persons of ordinary skill in the art will appreciate that the materials and thicknesses of the various layers will be similar to those disclosed with respect to the embodiment of FIG. 1.

In the embodiment shown in FIG. 3, substrate 12 is shown covered by insulating layer 14 and metal interconnect layer 16. As was the case with the embodiment illustrated in FIG. 1, persons of ordinary skill in the art will realize that FIG. 3 is merely illustrative and that metal interconnect layer 16 need not be the first metal interconnect layer in a multi-level metal integrated circuit.

Insulating layer 18, comprising, for example, deposited silicon dioxide, is disposed above metal interconnect layer 16 and includes a tungsten plug 20 formed in a via therethrough and electrically coupled to metal interconnect layer 16. As is known in the art, the upper surfaces of insulating layer 18 and tungsten plug 20 may be planarized to provide a relatively flat surface upon which to fabricate antifuse 50. Alternatively, tungsten plug 20 may be raised above the surface of the insulating layer 18 by performing planarization using CMP techniques or by performing a plasma oxide etch after planarization.

As previously mentioned, an antifuse material layer 22 is disposed over tungsten plug 20. Antifuse material layer 22 is the same as that disclosed with respect to the embodiment of FIG. 1. A barrier metal layer 24 such as Ta, TaN, TaC, Ti, TiC, or TiN having a thickness of about 25 nm to about 200 nm is disposed over the antifuse material layer forming an upper electrode of the antifuse 50 of FIG. 3. In the embodiment illustrated

in FIG. 3, an oxide layer 28 is deposited over the barrier metal layer 24. A layer of photoresist is deposited on the oxide layer and then oxide layer is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. The oxide layer 28 protects the antifuse material layer 22 from being removed during the photoresist stripping step. Since Al, Ti, Ta, TaN, TaC, TiC, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. Since the tungsten layer is thin, only a thin layer of photoresist is required to pattern the hard mask. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched in RIE with SF6 chemistry. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22.

A difference between the embodiments of FIGS. 1 and 3 is that an additional insulating layer 34, that may comprise a deposited layer silicon nitride or silicon oxide (using PECVD techniques) having a thickness of about 50 nm to about 200 nm, with about 100 nm preferred, may be employed over the structure including antifuse material layer 22 and barrier metal layer 24, as shown in FIG. 3. This material protects antifuse material layer 22 from shorting with the metal interconnect layer 26. Metal interconnect layer 26 is disposed over the insulating layer 34 and contacts barrier metal layer 24 through a via formed therethrough.

Referring now to FIG. 4, a cross-sectional view shows a fourth illustrative metal-to-metal antifuse 60. The embodiment illustrated in FIG. 4 is similar to the embodiment illustrated in FIG. 1, and structures in the embodiment of FIG. 4 corresponding to structures in FIG. 1 will be identified by the same reference numerals. Also, unless otherwise noted, persons of ordinary skill in the art will appreciate that the materials and thicknesses of the various layers will be similar to those disclosed with respect to the embodiment of FIG. 1.

In the embodiment shown in FIG. 4, substrate 12 is shown covered by insulating layer 14 and metal interconnect layer 16. As was the case with the embodiment illustrated in FIG. 1, persons of ordinary skill in the art will realize that FIG. 3 is merely illustrative and that metal interconnect layer 16 need not be the first metal interconnect layer in a multi-level

metal integrated circuit.

Insulating layer 18, comprising, for example, deposited silicon dioxide, is disposed above metal interconnect layer 16 and includes a tungsten plug 20 formed in a via therethrough and electrically coupled to metal interconnect layer 16. As is known in the art, the upper surfaces of insulating layer 18 and tungsten plug 20 may be planarized to provide a relatively flat surface upon which to fabricate antifuse 60. Alternatively, tungsten plug 20 may be raised above the surface of the insulating layer 18 by performing planarization using CMP techniques or by performing a plasma oxide etch after planarization.

As previously mentioned, an antifuse material layer 22 is disposed over tungsten plug 20. Antifuse material layer 22 is the same as that disclosed with respect to the embodiment of FIG. 1. A barrier metal layer 24 such as Ta, TaN, TaC, Ti, TiC, or TiN having a thickness of about 25 nm to about 200 nm is disposed over the antifuse material layer forming an upper electrode of the antifuse 60 of FIG. 4. In the embodiment illustrated in FIG. 4, an oxide layer 28 is deposited over the barrier metal layer 24. A layer of photoresist is deposited on the oxide layer and then oxide layer is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. The oxide layer 28 protects the antifuse material layer 22 from being removed during the photoresist stripping step. Since Al, Ti, Ta, TaC, TaN, TiC, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. Since the tungsten layer is thin, only a thin layer of photoresist is required to pattern the hard mask. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched in RIE with SF6 chemistry. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22.

A difference between the embodiments of FIGS. 1 and 4 is that an additional insulating layer or spacer 35, that may comprise a deposited layer of silicon nitride or silicon oxide (using PECVD techniques) having a thickness of about 50 nm to about 200 nm, with about 100 nm preferred, may be employed covering and adjacent to the structure including antifuse material layer 22 and barrier metal layer 24, as shown in FIG. 4. This material

protects antifuse material layer 22 from shorting with the metal interconnect layer 26. Metal interconnect layer 26 is disposed over the spacer 35 and contacts barrier metal layer 24, as illustrated in FIG. 4.

FIGS. 5A through 5C are cross-sectional views of the antifuse of FIG. 1 showing the structure existing at selected points in the fabrication process. Since the fabrication of antifuse 10 begins after the planarization of the insulating layer 18 and tungsten plug 20 that follows well-known prior processing steps, all of FIGS. 5A through 5C show the insulating layer 18 and tungsten plug 20 as the starting point for the fabrication process.

Referring first to FIG. 5A, antifuse 10 of FIG. 1 is fabricated by forming antifuse material layer 22 over tungsten plug 20 and insulating layer 18. As previously noted, if antifuse layer 22 is to be formed from a layer of amorphous carbon or doped amorphous carbon, a thin adhesion-promoting material layer such as SiN or SiC (shown in FIG. 2 at reference numeral 36) is deposited using PECVD techniques.

Antifuse layer 22 is then deposited using PECVD techniques. As will be appreciated by persons of ordinary skill in the art, the thickness of antifuse material layer 22 is usually from about 10 nm to about 80 nm. Such skilled persons will realize that the thickness used will depend on the desired programming voltage for the finished antifuse. If necessary, a thin adhesion-promoting material layer 38 is then deposited over the antifuse material layer 22 to provide adhesion for the overlying barrier metal layer to be deposited.

Next, barrier metal layer 24 is deposited to a thickness of about 25 nm to about 200 nm using PVD sputtering techniques. Then oxide layer 28 is deposited over the barrier metal layer 24. The oxide layer 28 is deposited at about 500 angstroms to about 4,000 angstroms, with about 2,000 angstroms preferred. A layer photoresist is deposited on the oxide layer 28 and then oxide layer 28 is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. Since Al, Ti, TiC, Ta, TaC, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. The tungsten layer 28 can be deposited at about 250 angstroms to about 4,000 angstroms, with about 500 angstroms preferred. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten

hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22. FIG. 5A depicts the partially-completed antifuse structure after the deposition of barrier metal layer 24 and the oxide or tungsten layer 28.

After antifuse material layer, any necessary adhesion layers, and barrier metal layer 24 and oxide or tungsten hard mask have been formed, a masking layer 40 is formed over the surface of barrier metal layer 24 to define the shape of the antifuse "stack" comprising layers 36, 22, 38, and 24. A conventional etching step is then performed to etch the antifuse stack to the desired geometry. FIG. 5B depicts the structure remaining after the etching step used to define the shape of the antifuse stack but prior to removal of the masking layer 40.

Referring now to FIG. 5C, masking layer 40 is removed using conventional mask-stripping steps. An oxide layer (not shown) is formed and defined to protect the sides of the antifuse stack and a metal interconnect layer 26 is deposited over the layers 36, 22, 38, and 24 comprising the antifuse stack, the upper surface of the oxide layer (not shown), and the exposed surface of the insulating layer 18. A masking layer 42 is formed over metal interconnect layer 26 using conventional photolithographic techniques in preparation for a metal-etch step to define the geometry of metal interconnect layer 26. FIG. 5C depicts the structure existing after forming masking layer 42 but prior to the metal etching step. FIG. 1 depicts the antifuse structure after performance of the metal etching step. As was previously noted, an insulating layer (not shown) may be first deposited over barrier layer 24, a contact via is then formed therein, and metal interconnect layer 26 is then deposited over the insulating layer and in the contact via.

Referring now to FIGS. 6A through 6C, cross-sectional views show the structure of the antifuse 30 of FIG. 2 existing at selected points in the fabrication process. As the process depicted in FIGS. 5A through 5C, the fabrication process for antifuse 30 begins after the planarization of the insulating layer 18 and tungsten plug 20 (or raising of the tungsten plug 20) that follows well-known prior processing steps. Therefore, all of FIGS. 6A through 6C show the insulating layer 18 and tungsten plug 20 as the starting point for the fabrication process.

Referring first to FIG. 6A, antifuse 30 of FIG. 1 is fabricated by depositing barrier metal layer 32 over tungsten plug 20 and insulating layer 18. Antifuse material layer 22 is then deposited over barrier metal layer 32. As previously noted, if antifuse layer 22 is to be formed from a layer of amorphous carbon or doped amorphous carbon, a thin adhesion-

promoting material layer such as SiN or SiC (shown in FIG. 6A at reference numeral 36) is deposited using PECVD techniques.

Antifuse layer 22 is then deposited using PECVD techniques. As will be appreciated by persons of ordinary skill in the art, the thickness of antifuse material layer 22 is usually from about 10 nm to about 80 nm. Such skilled persons will realize that the thickness used in an actual embodiment disposed on an integrated circuit will depend on the desired programming voltage for the finished antifuse. For example, an antifuse fabricated with such an antifuse layer having a thickness of about 20 nm will require about 5 volts for programming. If necessary, a thin adhesion-promoting material layer 38 is then deposited over the antifuse material layer to provide adhesion for the overlying barrier metal layer to be deposited.

Next, barrier metal layer 24 is deposited to a thickness of about 25 nm to about 200 nm using PVD techniques. Then oxide layer 28 is deposited over the barrier metal layer 24. The oxide layer 28 is deposited at about 500 angstroms to about 4,000 angstroms, with about 2,000 angstroms preferred. A layer of photoresist is deposited on the oxide layer 28 and then oxide layer 28 is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. Since Al, Ti, TiC, Ta, TaC, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. The tungsten layer 28 can be deposited at about 250 angstroms to about 4,000 angstroms, with about 500 angstroms preferred. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22. FIG. 6A depicts the partially-completed antifuse structure after the deposition of barrier metal layer 24 and the oxide or tungsten layer 28.

After antifuse material layer, any necessary adhesion layers, and barrier metal layer 24 and oxide or tungsten hard mask have been formed, a masking layer 40 is formed over the surface of barrier metal layer 24 to define the shape of the antifuse "stack" comprising layers 32, 36, 22, 38, and 24. A conventional etching step is then performed to etch the antifuse

stack to the desired geometry. FIG. 6B depicts the structure remaining after the etching step used to define the shape of the antifuse stack but prior to removal of the masking layer 40.

Referring now to FIG. 6C, masking layer 40 is removed using conventional mask-stripping steps and an insulating layer 34 is deposited over the layers 36, 22, 38, and 24 comprising the antifuse stack and the exposed surface of the insulating layer 18. Conventional masking and etching techniques (not shown) are then employed to form a contact via in insulating layer 34. Next, metal interconnect layer 26 is deposited over insulating layer 34 and in the contact via where it is electrically connected to barrier metal layer 24. A masking layer 42 is formed over metal interconnect layer 26 using conventional photolithographic techniques in preparation for a metal-etch step to define the geometry of metal interconnect layer 26. FIG. 6C depicts the structure existing after forming masking layer 42 but prior to the metal etching step. FIG. 2 depicts the structure of antifuse 30 after performance of the metal etching step.

Referring now to FIGS. 7A through 7C, cross-sectional views show the structure of the antifuse 50 of FIG. 3 existing at selected points in the fabrication process. As the process depicted in FIGS. 5A through 5C, the fabrication process for antifuse 50 begins after the planarization of the insulating layer 18 and tungsten plug 20 (or raising of the tungsten plug 20) that follows well-known prior processing steps. Therefore, all of FIGS. 7A through 7C show the insulating layer 18 and tungsten plug 20 as the starting point for the fabrication process.

Referring first to FIG. 7A, antifuse 50 of FIG. 3 is fabricated by depositing antifuse material layer 22 over tungsten plug 20 and insulating layer 18. As previously noted, if antifuse layer 22 is to be formed from a layer of amorphous carbon or doped amorphous carbon, a thin adhesion-promoting material layer such as SiN or SiC (shown in FIG. 7A at reference numeral 36) is deposited using PECVD techniques.

Antifuse layer 22 is then deposited using PECVD techniques. As will be appreciated by persons of ordinary skill in the art, the thickness of antifuse material layer 22 is usually from about 10 nm to about 80 nm. Such skilled persons will realize that the thickness used in an actual embodiment disposed on an integrated circuit will depend on the desired programming voltage for the finished antifuse. For example, an antifuse fabricated with such an antifuse layer having a thickness of about 20 nm will require about 5 volts for programming. If necessary, a thin adhesion-promoting material layer 38 is then deposited over the antifuse material layer to provide adhesion for the overlying barrier metal layer to

be deposited.

Next, barrier metal layer 24 is deposited to a thickness of about 25 nm to about 200 nm using PVD techniques. Then oxide layer 28 is deposited over the barrier metal layer 24. The oxide layer 28 is deposited at about 500 angstroms to about 4,000 angstroms, with about 2,000 angstroms preferred. A layer of photoresist is deposited on the oxide layer 28 and then oxide layer 28 is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. Since Al, Ti, TiC, Ta, TaC, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. The tungsten layer 28 can be deposited at about 250 angstroms to about 4,000 angstroms, with about 500 angstroms preferred. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22. FIG. 7A depicts the partially-completed antifuse structure after the deposition of barrier metal layer 24 and the oxide or tungsten layer 28.

After antifuse material layer 22, any necessary adhesion layers, and barrier metal layer 24 and oxide or tungsten hard mask have been formed, a masking layer 40 is formed over the surface of barrier metal layer 24 to define the shape of the antifuse "stack" comprising layers 36, 22, 38, and 24. A conventional etching step is then performed to etch the antifuse stack to the desired geometry. FIG. 7B depicts the structure remaining after the etching step used to define the shape of the antifuse stack but prior to removal of the masking layer 40.

Referring now to FIG. 7C, masking layer 40 is removed using conventional mask-stripping steps and an insulating layer 34 is deposited over the layers 36, 22, 38, and 24 comprising the antifuse stack and the exposed surface of the insulating layer 18. Conventional masking and etching techniques (not shown) are then employed to form a contact via in insulating layer 34. Next, metal interconnect layer 26 is deposited over insulating layer 34 and in the contact via where it is electrically connected to barrier metal layer 24. A masking layer 42 is formed over metal interconnect layer 26 using conventional photolithographic techniques in preparation for a metal-etch step to define the geometry of

metal interconnect layer 26. FIG. 7C depicts the structure existing after forming masking layer 42 but prior to the metal etching step. FIG. 3 depicts the structure of antifuse 50 after performance of the metal etching step.

Referring now to FIGS. 8A through 8C, cross-sectional views show the structure of the antifuse 60 of FIG. 4 existing at selected points in the fabrication process. As the process depicted in FIGS. 5A through 5C, the fabrication process for antifuse 60 begins after the planarization of the insulating layer 18 and tungsten plug 20 (or raising of the tungsten plug 20) that follows well-known prior processing steps. Therefore, all of FIGS. 8A through 8C show the insulating layer 18 and tungsten plug 20 as the starting point for the fabrication process.

Referring first to FIG. 8A, antifuse 60 of FIG. 4 is fabricated by depositing antifuse material layer 22 over tungsten plug 20 and insulating layer 18. As previously noted, if antifuse layer 22 is to be formed from a layer of amorphous carbon or doped amorphous carbon, a thin adhesion-promoting material layer such as SiN or SiC (shown in FIG. 8A at reference numeral 36) is deposited using PECVD techniques.

Antifuse layer 22 is then deposited using PECVD techniques. As will be appreciated by persons of ordinary skill in the art, the thickness of antifuse material layer 22 is usually from about 10 nm to about 80 nm. Such skilled persons will realize that the thickness used in an actual embodiment disposed on an integrated circuit will depend on the desired programming voltage for the finished antifuse. For example, an antifuse fabricated with such an antifuse layer having a thickness of about 20 nm will require about 5 volts for programming. If necessary, a thin adhesion-promoting material layer 38 is then deposited over the antifuse material layer to provide adhesion for the overlying barrier metal layer to be deposited.

Next, barrier metal layer 24 is deposited to a thickness of about 25 nm to about 200 nm using PVD techniques. Then oxide layer 28 is deposited over the barrier metal layer 24. The oxide layer 28 is deposited at about 500 angstroms to about 4,000 angstroms, with about 2,000 angstroms preferred. A layer of photoresist is deposited on the oxide layer 28 and then oxide layer 28 is etched. Following etching, the photoresist is stripped and the remaining oxide layer is left as a hard mask, acting as an etch mask when etching the barrier metal layer 24 and the antifuse material layer 22. Since Al, Ti, TiC, Ta, TaC, TaN, and TiN have high selectivity to tungsten (W), a thin layer of PVD or CVD tungsten (about 25 nm to about 50 nm) can also be used as a hard mask 28 to etch the underlying metal 24. The tungsten

layer 28 can be deposited at about 250 angstroms to about 4,000 angstroms, with about 500 angstroms preferred. Once the hard mask is open, the remaining photoresist is stripped and metal layer 24 can be etched without organic material present on the metal stack. Once the metal layer 24 is etched, the tungsten hard mask can be etched. It is also possible to leave the thin tungsten layer above the etched metal stack. The oxide or tungsten hard mask provides high etch selectivity and the possibility to etch metals without affecting the dielectric constant value (K) and mechanical properties of the amorphous carbon antifuse material layer 22. FIG. 8A depicts the partially-completed antifuse structure after the deposition of barrier metal layer 24 and oxide or tungsten layer 28.

After antifuse material layer 22, any necessary adhesion layers, and barrier metal layer 24 and oxide or tungsten hard mask have been formed, a masking layer 40 is formed over the surface of barrier metal layer 24 to define the shape of the antifuse "stack" comprising layers 36, 22, 38, and 24. A conventional etching step is then performed to etch the antifuse stack to the desired geometry. FIG. 8B depicts the structure remaining after the etching step used to define the shape of the antifuse stack but prior to removal of the masking layer 40.

Referring now to FIG. 8C, masking layer 40 is removed using conventional mask-stripping steps and an insulating layer 35 is deposited over the layers 36, 22, 38, and 24 comprising the antifuse stack and the exposed surface of the insulating layer 18. Conventional masking and etching techniques (not shown) are then employed to form insulating layer 35 into spacers. Next, metal interconnect layer 26 is deposited over spacers 35 and is electrically connected to barrier metal layer 24. A masking layer 42 is formed over metal interconnect layer 26 using conventional photolithographic techniques in preparation for a metal-etch step to define the geometry of metal interconnect layer 26. FIG. 8C depicts the structure existing after forming masking layer 42 but prior to the metal etching step. FIG. 4 depicts the structure of antifuse 60 after performance of the metal etching step.

The use of amorphous carbon, amorphous carbon doped with at least one of hydrogen and fluorine, or amorphous silicon carbide, as the antifuse material layer in metal-to-metal antifuses inhibits the "healing" or "switching" by which the conductive filament deteriorates after programming.

While the invention has been described with reference to an exemplary embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the

invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A metal-to-metal antifuse disposed between two metal interconnect layers in an integrated circuit and comprising:

a tungsten plug disposed in a via in an insulating layer disposed above and in electrical contact with a lower metal interconnect layer;

an antifuse material layer disposed above an upper surface of said tungsten plug, said antifuse material layer selected from a group comprising at least one of amorphous carbon, amorphous carbon doped with at least one of hydrogen and fluorine, and amorphous silicon carbide;

a layer of a barrier metal disposed over said antifuse material layer; and

an upper electrode disposed over said layer of a barrier metal.

2. The metal-to-metal antifuse of Claim 1, wherein said antifuse material layer comprises a layer of amorphous carbon disposed between two layers of an adhesion-promoting material.

3. The metal-to-metal antifuse of Claim 2 wherein said layer of amorphous carbon is doped with at least one of hydrogen and fluorine.

4. The metal-to-metal antifuse of Claim 1, further comprising a second insulating layer disposed over and in physical contact with said layer of barrier metal, said antifuse material layer, and said insulating layer.

5. The metal-to-metal antifuse of Claim 1, further comprising a spacer disposed in physical contact with said antifuse material layer.

6. The metal-to-metal antifuse of Claim 1, wherein said antifuse material layer is about 10 nm to about 80 nm in thickness.

7. The metal-to-metal antifuse of Claim 1, wherein said barrier metal layer is about 25 nm to about 200 nm in thickness.

8. The metal-to-metal antifuse of Claim 1, wherein said barrier metal layer is from a material selected from the group comprising Ta, TaC, TaN, Ti, TiC, and TiN.

9. The metal-to-metal antifuse of Claim 1, wherein said antifuse material layer is formed from a first layer of amorphous silicon carbide, a second layer of amorphous carbon, and a third layer of amorphous silicon carbide.

10. The metal-to-metal antifuse of Claim 1, wherein said antifuse material layer is formed from a first layer of amorphous silicon nitride, a second layer of amorphous carbon, and a third layer of amorphous silicon nitride.

11. The metal-to-metal antifuse of Claim 1, further comprising an oxide layer disposed on said barrier metal layer.

12. The metal-to-metal antifuse of Claim 1, further comprising a tungsten layer disposed on said barrier metal layer.

13. A metal-to-metal antifuse disposed between two metal interconnect layers in an integrated circuit and comprising:

a tungsten plug disposed in a via in an insulating layer disposed above and in electrical contact with a lower metal interconnect layer;

a first layer of barrier metal disposed above and in electrical contact with said tungsten plug;

an antifuse material layer disposed above said first layer of barrier material, said antifuse material layer selected from a group comprising at least one of amorphous carbon, amorphous carbon doped with at least one of hydrogen and fluorine, and amorphous silicon carbide;

a second layer of a barrier metal disposed over said antifuse material layer;

a second insulating layer disposed over said first insulating layer, said antifuse material layer, said first layer of a barrier metal, and said second layer of a barrier metal; and

an upper electrode disposed over said second layer of a barrier metal.

14. The metal-to-metal antifuse of Claim 13, wherein said antifuse material layer comprises a layer of amorphous carbon disposed between two layers of an adhesion-promoting material.

15. The metal-to-metal antifuse of Claim 14, wherein said layer of amorphous carbon is doped with at least one of hydrogen and fluorine.

16. The metal-to-metal antifuse of Claim 13, further comprising a spacer disposed in physical contact with said antifuse material layer.

17. The metal-to-metal antifuse of Claim 13, wherein said antifuse material layer is about 10 nm to about 80 nm in thickness.

18. The metal-to-metal antifuse of Claim 13, wherein said barrier metal layer is about 25 nm to about 200 nm in thickness.

19. The metal-to-metal antifuse of Claim 13, wherein said barrier metal layer is from a material selected from the group comprising Ta, TaC, TaN, Ti, TiC, and TiN.

20. The metal-to-metal antifuse of Claim 13, wherein said antifuse material layer is formed from a first layer of amorphous silicon carbide, a second layer of amorphous carbon, and a third layer of amorphous silicon carbide.

21. The metal-to-metal antifuse of Claim 13, wherein said antifuse material layer is formed from a first layer of amorphous silicon nitride, a second layer of amorphous carbon, and a third layer of amorphous silicon nitride.

22. The metal-to-metal antifuse of Claim 13, further comprising an oxide layer disposed on said second layer of a barrier metal layer.

23. The metal-to-metal antifuse of Claim 13, further comprising a tungsten layer disposed on said second layer of a barrier metal layer.

24. A method of fabricating a metal-to-metal antifuse, comprising:

planarizing an insulating layer and a tungsten plug;

forming an antifuse material layer over said insulating layer and said tungsten plug, wherein said antifuse material layer is selected from the group comprising amorphous carbon, amorphous carbon doped with at least one of hydrogen and fluorine, and amorphous silicon carbide;

defining said antifuse material layer;

forming a barrier metal layer over said antifuse material layer;

defining said barrier metal layer;

forming an oxide or tungsten layer over said barrier metal layer;

forming a layer of photoresist over said oxide or said tungsten layer;

defining said oxide or said tungsten layer;

removing said photoresist;

forming a first masking layer over said barrier metal layer;

defining a shape of said antifuse;

removing said first masking layer;

forming a metal interconnect layer over said insulating layer;

forming a second masking layer over said metal interconnect layer; and

removing said second masking layer.

25. The method of Claim 24, wherein said forming said antifuse material layer comprises forming said antifuse material layer to a thickness of from about 10 nm to about 80 nm.

26. The method of Claim 24, wherein said forming said barrier metal layer comprises forming said barrier metal layer to a thickness of from about 25 nm to about 200 nm.

27. The method of Claim 24, wherein said forming said barrier metal layer comprises forming said barrier metal layer from a material selected from the group comprising Ta, TaC, TaN, Ti, TiC, and TiN.

28. The method of Claim 24, further comprising forming a second insulating layer in physical contact with said layer of barrier metal, said antifuse material layer; said insulating layer; and said metal interconnect layer; and defining said second insulating material.

29. The method of Claim 24, further comprising forming a layer of a third insulating material over said barrier metal layer and said antifuse material layer; and defining said third insulating material into spacers disposed in physical contact with said antifuse material layer and said barrier metal layer.

30. The method of Claim 24, further comprising disposing adhesion layers in physical contact with said antifuse material layer and said layer of barrier metal.

31. The method of Claim 24, wherein said forming said antifuse material layer comprises forming a first layer of amorphous silicon carbide, a second layer of amorphous carbon, and a third layer of amorphous silicon carbide.

32. The method of Claim 24, wherein said forming said antifuse material layer comprises forming a first layer of amorphous silicon nitride, a second layer of amorphous carbon, and a third layer of amorphous silicon nitride.

33. The method of Claim 24, wherein said forming an antifuse material layer is deposited from an acetylene source gas.

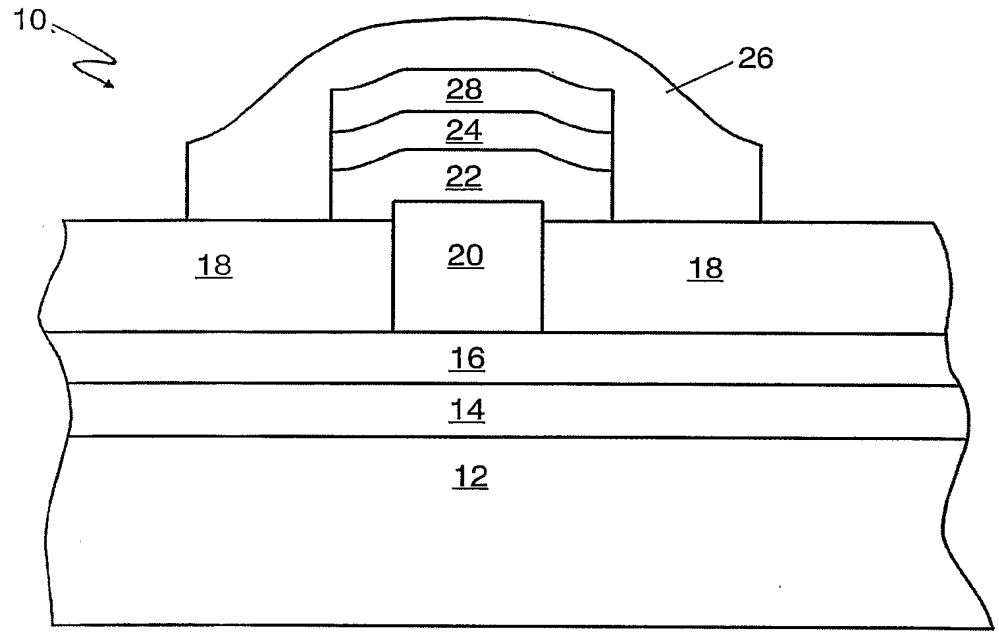
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FIG. 1

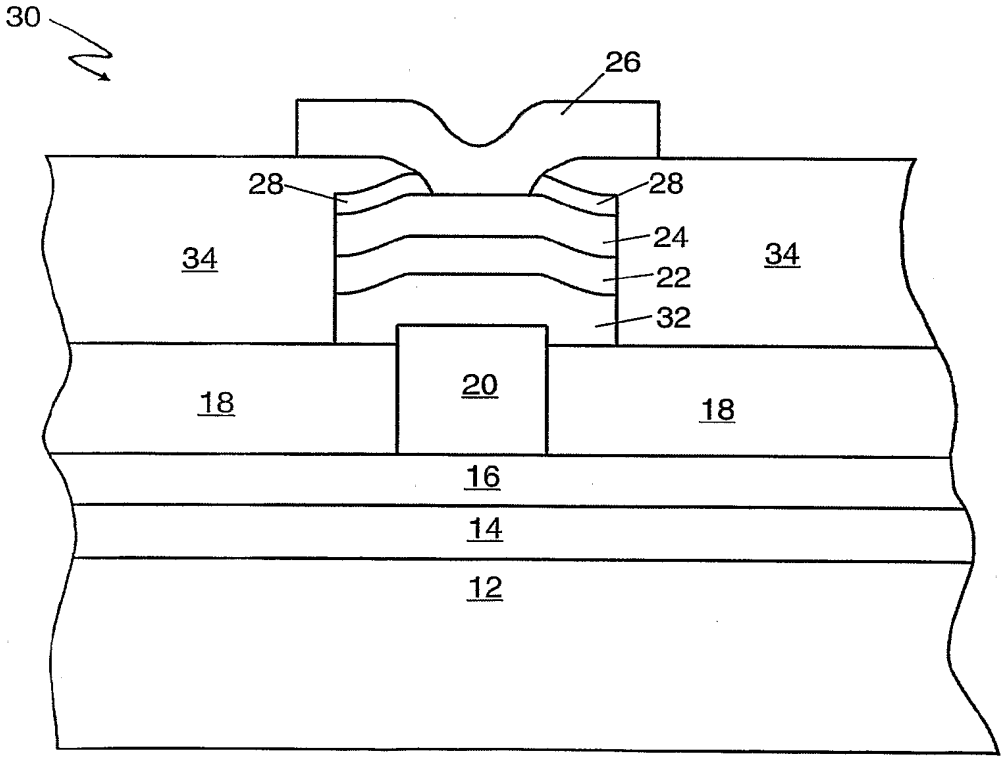
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FIG. 2

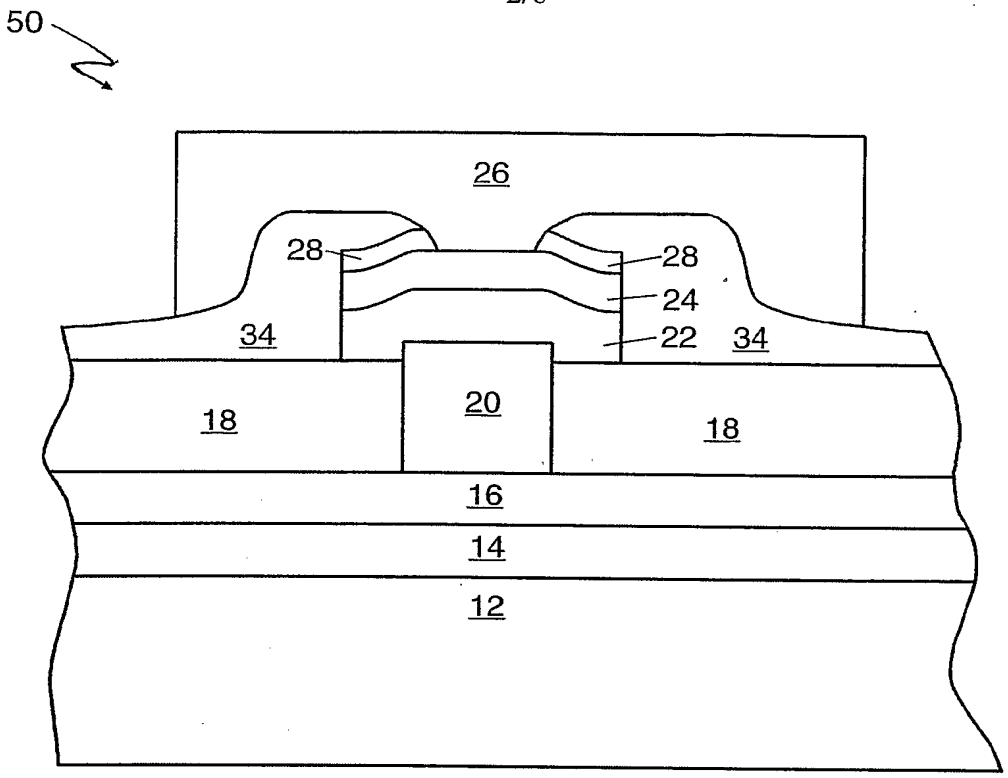
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FIG. 3

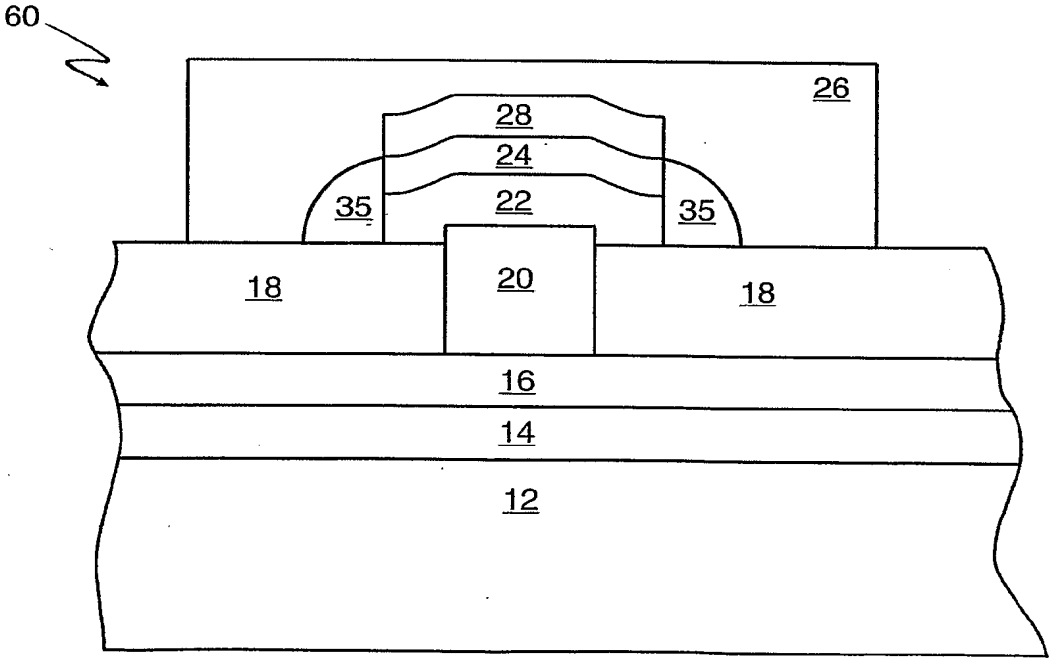
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FIG. 4

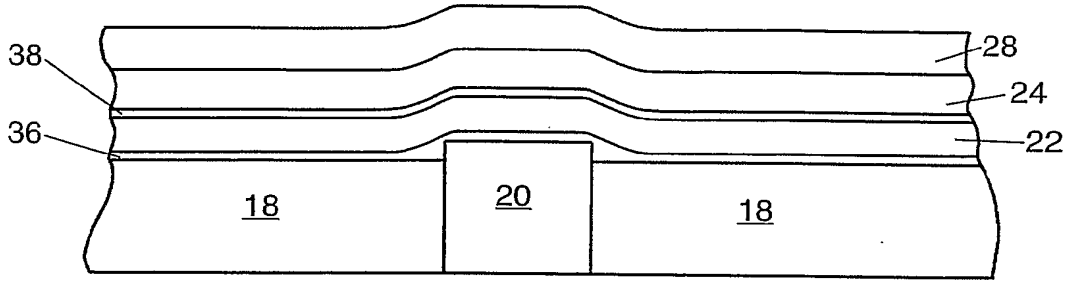

FIG. 5A

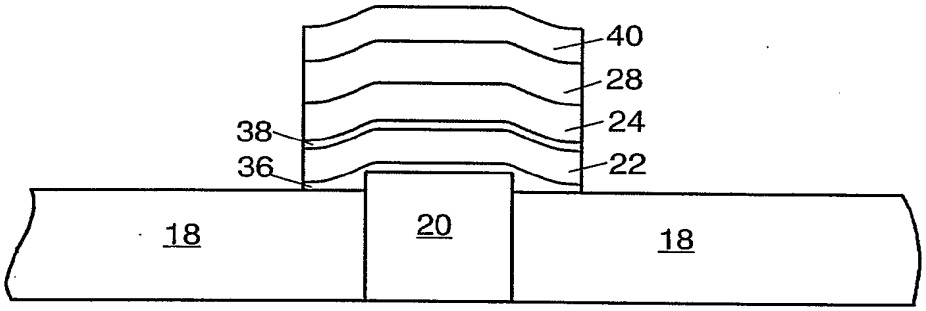

FIG. 5B

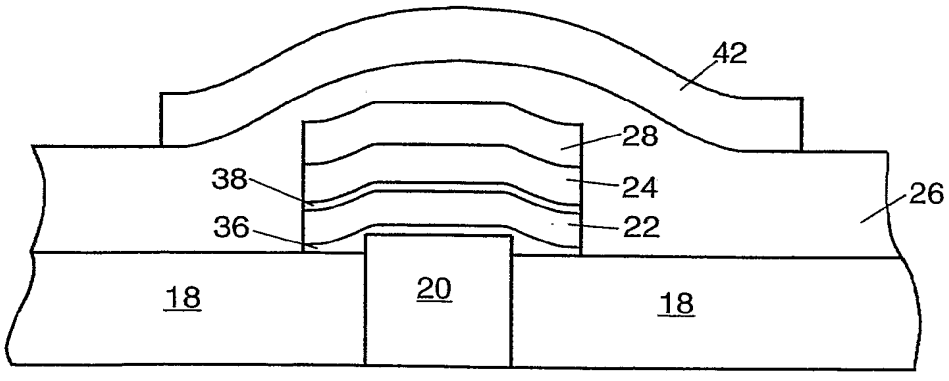

FIG. 5C

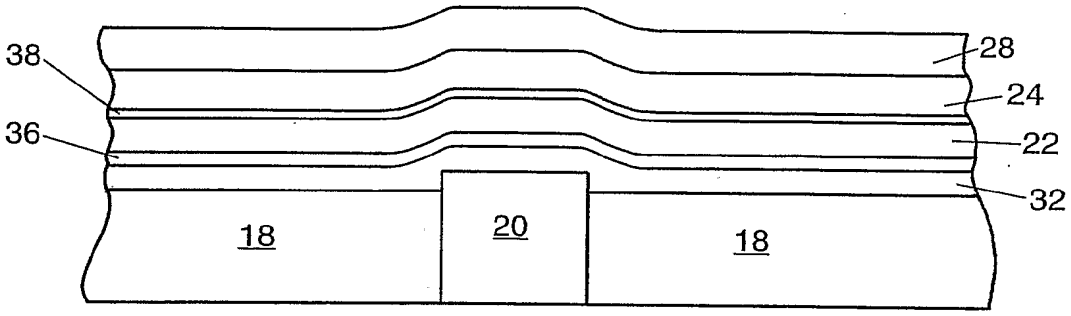

FIG. 6A

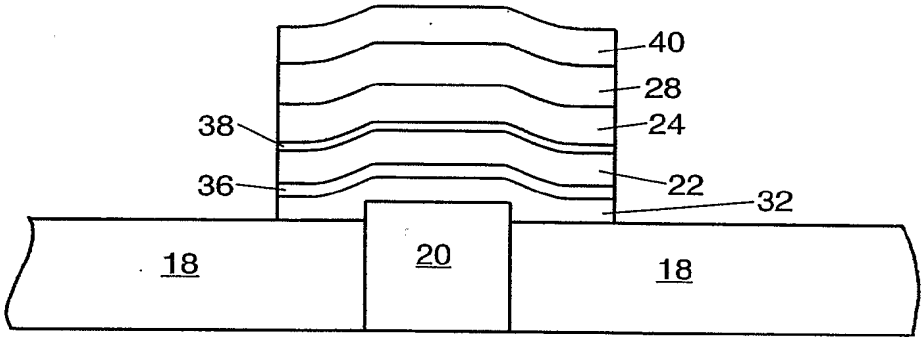

FIG. 6B

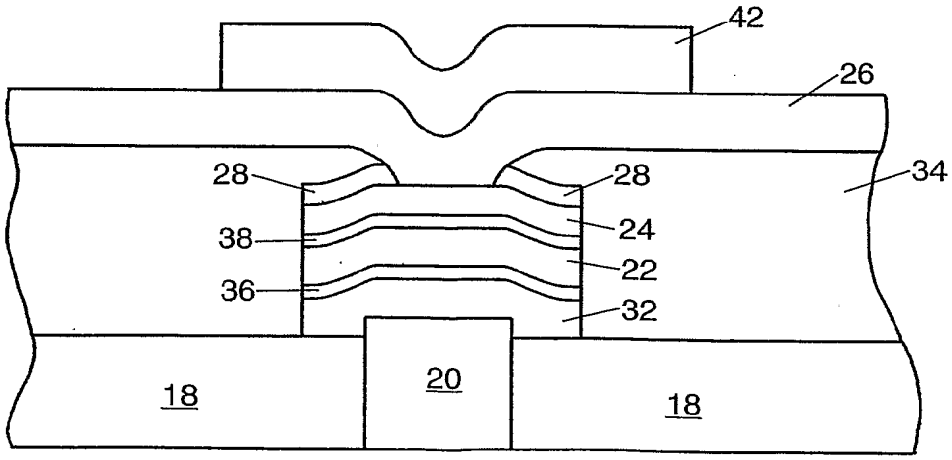

FIG. 6C

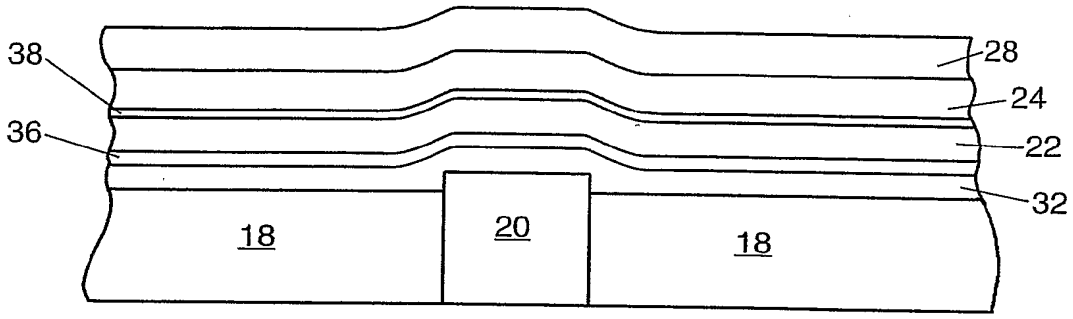

FIG. 7A

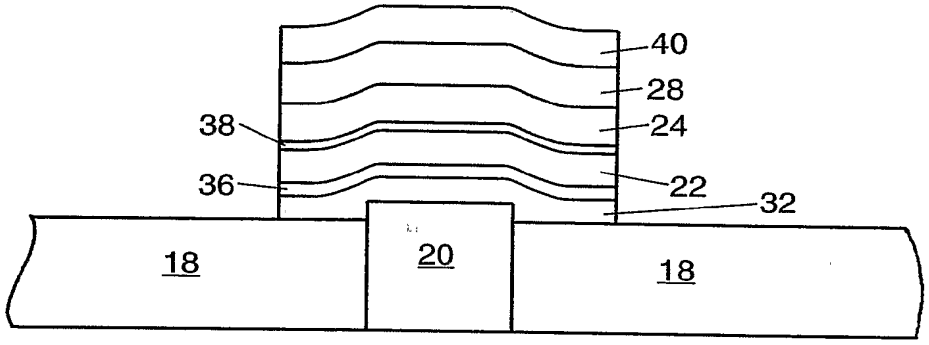

FIG. 7B

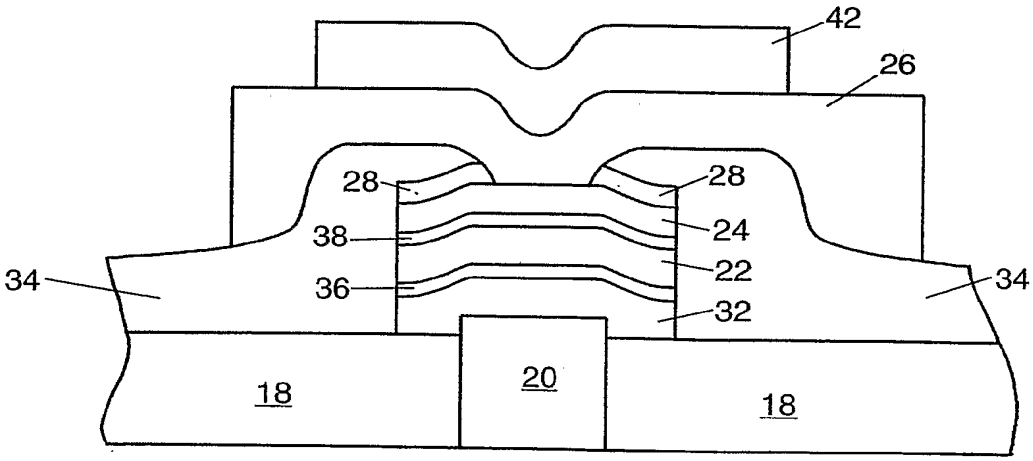

FIG. 7C

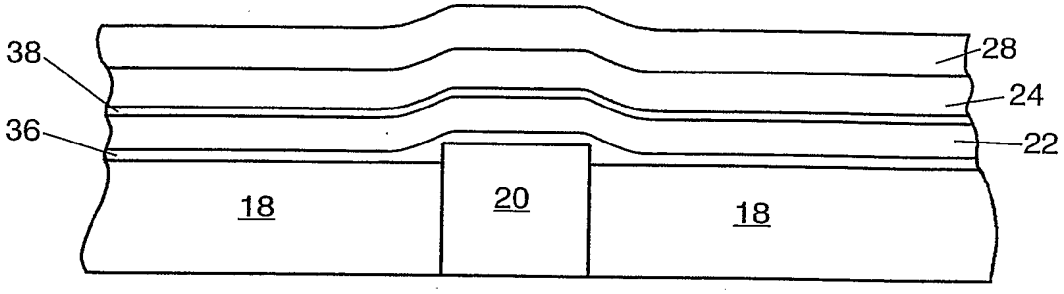

FIG. 8A

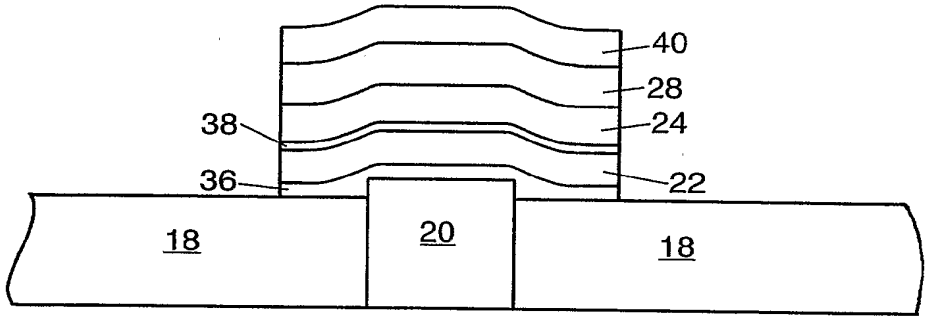

FIG. 8B

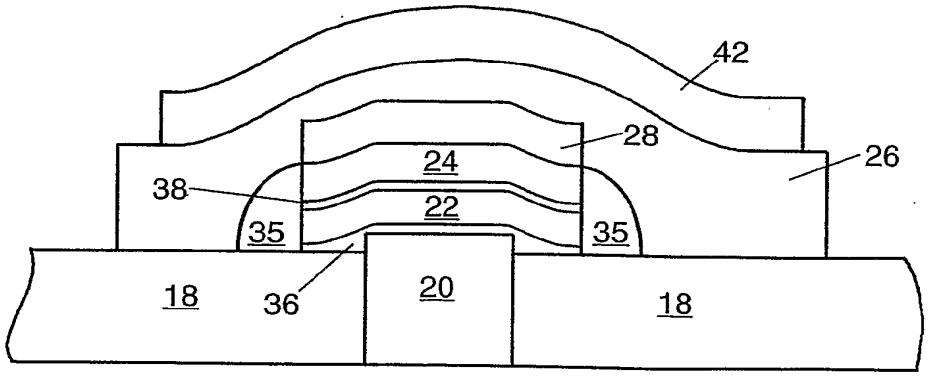

FIG. 8C